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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/815,446	03/22/2001	Christopher A. Bode	2000.068000/TT4149	7640
23720	7590	12/17/2004	EXAMINER	
WILLIAMS, MORGAN & AMERSON, P.C. 10333 RICHMOND, SUITE 1100 HOUSTON, TX 77042			GARCIA OTERO, EDUARDO	
			ART UNIT	PAPER NUMBER
			2123	

DATE MAILED: 12/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

09/815,446

**Applicant(s)**

BODE ET AL.

**Examiner**

Eduardo Garcia-Otero

**Art Unit**

2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 07 October 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-33 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-33 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 March 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

**DETAILED ACTION: Final Action**

***Introduction***

1. Title is: METHOD AND APPARATUS FOR PERFORMING FIELD-TO-FIELD COMPENSATION.
2. First named inventor is: BODE.
3. Claims 1-33 have been submitted, examined, and rejected.
4. US non-provisional application was filed 3/22/2001, and no earlier priority is claimed.
5. Applicant's Amendment was received 10/7/04.

***Index of Important Prior Art***

6. Conrad refers to US patent 6,528,219.
7. Su refers to US patent 6,456,736.
8. Drohan refers to US patent 6,594,002.

***Definitions***

9. “**Metrology**” is defined as “The science of measurement for determination of conformance to technical requirements including the development of standards and systems for absolute and relative measurements” by The Authoritative Dictionary of IEEE Standards and Terms, Seventh Edition, by IEEE Press, ISBN 0-7381-2601-2, 2000.

***Claim Interpretations***

10. “**Semiconductor device**” is interpreted as devices such as integrated circuits made on wafers, see FIG 2.
11. “**Metrological data**” in claim 1 is interpreted broadly as “measured data”. Note broad discussion at Specification bottom of page 8 and top of page 9 ( “... and the like”).
12. “**Field-to-field**” in claim 1 is interpreted as multiple exposure fields in a single wafer, see elements 210a and 210b in FIG 2, and see specification page 11. Also see page 7 “Wafer-to-wafer, wafer-lot to wafer-lot, and even field-to-field (portions of a wafer)”.
13. Note that wafer-lot to wafer-lot appears to refer to “a lot-mean sized set... mean value for an entire manufacturing lot of semiconductor wafers” per Specification page 12 line 18. It is not clear whether a “lot” refers to a set of wafers cut from a single crystal, or a set of wafers cut from a simultaneously grown set of crystals.

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14. **“Wafer-mean error”** in claim 1 is interpreted as “A wafer-mean error data set relates the average overlay error for a particular wafer as a whole from one process to the other” at page 14 line 13.
15. **“Field-mean error”** in claim 1 is interpreted as “field-mean error data corresponds to the average overlay error relating to a particular field from one process to another” at page 14 line 14.
16. **“Comparing”** in claim 1 is interpreted as page 14 line 22 “calculation of the difference in the wafer-mean error to the field-mean error... determine whether significance residual error exists... compared to a pre-determined threshold tolerance... When a determination is made that no significant residual error exists in any particular exposure field 210, the wafer-mean overlay is used” and page 15 line 8 “When a determination is made that significant residual error exists... the system uses field-level, or field-mean, error data to adjust or compensate for the exposure field 210 error”.
17. **“Predetermined amount of residual error”** is interpreted as “pre-determined threshold tolerance” per page 14 line 25.

***Applicant's Remarks***

18. Applicant persuasively asserts that the amended claims have overcome all prior objections and rejections.
19. However, new 35 USC 112 rejections are provided below for the amended claims.

***35 USC § 112- first paragraph- enablement***

20. The following is a quotation of the first paragraph of 35 U.S.C. 112: The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
21. Claims 1-33 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

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22. In claim 1, the term **“predetermined amount of residual error”** is not enabled. There is not adequate discussion in the Specification to enable predetermining the threshold amount of residual error that determines whether field-level adjustments are made, or whether wafer-level adjustments are made. See Specification page 14 line 25 “pre-determined threshold tolerance”.
23. In claim 1, the term **“performing at least one of a field-level adjustment and a wafer-level adjustment based upon said residual-error analysis”** is not enabled. Note that according to the specification, the only one type of adjustment is allowed, based upon the whether or not the Specification page 14 line 25 “pre-determined threshold tolerance” is exceeded or not.
24. Claims 2-33 are not enabled for the same reasons as claim 1.

***35 USC § 112-Second Paragraph-indefinite claims***

25. The following is a quotation of the second paragraph of 35 U.S.C. 112: The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
26. Claims 1-33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
27. In claim 1, the term **“predetermined amount of residual error”** is not clear. There is not adequate discussion in the Specification regarding predetermining the threshold amount of residual error, that determines whether field-level adjustments are made, or whether wafer-level adjustments are made. See Specification page 14 line 25 “pre-determined threshold tolerance”.
28. Claims 2-33 are not enabled for the same reasons as claim 1.
29. Also, in claim 33, which depends from claim 1, the term “further comprising processing at least one additional semiconductor device” is not clear. The term “processing at least one semiconductor device” in independent claim appears to refer to processing at least multiple wafers (wafer-mean error), and each wafer has multiple fields (field-mean error). Thus, it is not clear how claim 1 could refer to just one semiconductor device. Thus, it is not clear how

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claim 33 further limits parent claim 1. Perhaps the definition of "semiconductor device" is not clear in the context of wafers and fields.

**Response to Amendments or new IDS-FINAL OFFICE ACTION**

30. Applicant's amendments or new IDS necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

***Patentable material***

31. At present, the Examiner believes that this application contains some potentially patentable material. Specifically, the prior art does not disclose Specification page 14 line 22 "calculation of the difference in the wafer-mean error to the field-mean error... determine whether significance residual error exists... compared to a pre-determined threshold tolerance... When a determination is made that no significant residual error exists in any particular exposure field 210, the wafer-mean overlay is used" and page 15 line 8 "When a determination is made that significant residual error exists... the system uses field-level, or field-mean, error data to adjust or compensate for the exposure field 210 error".
32. The prior art of record does disclose "within-field data variation plus a field-to-field variation" at Conrad column 3 line 59.

***Additional Cited Prior Art***

33. The following US patents or publications are hereby cited as prior art, but have not been used for rejection. Applicant should review these carefully before responding to this office action. Drohan discloses "wafer mean" at Abstract, and "residual errors" at column 1 line 53.

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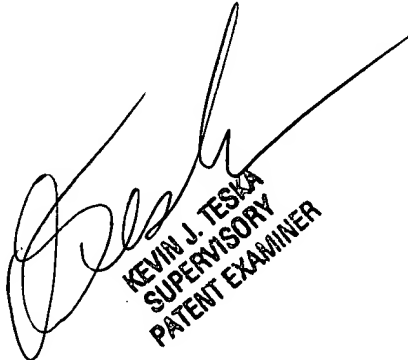
***Conclusion***

34. All pending claims stand rejected.

***Communication***

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 571-272-3711. The examiner can normally be reached on Monday through Thursday from 9:00 AM to 8:00 PM. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at 571-272-3761. The fax phone number for this group is 703-872-9306.

\* \* \* \* \*

  
KEVIN J. TESKA  
SUPERVISORY  
PATENT EXAMINER